TRL

TRL might be used to de-embed the DUT on a PCB fixture. This method would require a connectorized Thru line with a length equal to the input and output traces from the DUT to be created. Then another connectorized line like the thru but longer by 90 degrees, the match line, would be added. Lastly, two connectors would be added, simply shorted to ground. These are the Reflects. If the delay of the Thru is set to zero in the VNA calibration kit definition, then after calibration, the reference plane will be set in the middle of the Thru. Subsequent measurements of the DUT will then be referenced to the DUT input and output pins.

There are two issues with this sort of calibration technique. First, the match line will only be useable where it is 20 degrees to 160 degrees longer than the Thru at any given frequency. The useable bandwidth of the fixture will therefore be confined to between 0.22 * Fc and 1.78 * Fc, where Fc is the center frequency where the match line is exactly 90 degrees longer than the Thru line.

Secondly, the match line must have pristine Return Loss, better than 25 dB, including connector reflections. The Return Loss of this line sets the “floor” for Return Loss measurement of the DUT. Return Loss measurements which appear to be less than the Return Loss of the match line would be meaningless.

SOLT

It is also possible to create Open, Short, Load, and Thru artifacts on a PCB fixture. The Open and Short standards will have lead-in lines if the traces connect to the input and output of the DUT to set the reference plane properly. Normally, the calibration kit definitions entered in the VNA for a homemade calibration kit like this would use default entries that assume no Open capacitance, no Short inductance, a perfect 50Ω Load, and a Thru. These assumptions might hold to 1 or 2 GHz. The Short inductance can be made quite small, and the Thru can be accommodated using the unknown Thru technique, so its loss is not terribly important. The Open will have some fringing fields at the endpoint, though, which amounts to a capacitance that introduces some error. The Load will be very difficult to produce on a circuit board. A Return Loss of at least 30 dB is necessary, which is extremely difficult to attain. The best implementation might use four 0402, 200Ω Ohm resistors at the end of a trace, two perpendicular and the other two angled off the end. This reduces lead inductance which still exists, even in 0402 resistors. At the same time, the capacitance to ground from the connection pad is a problem.

SOLT is a viable alternative for calibration on a PCB, but the design is quite difficult and will likely only be suitable to a few gigahertz of bandwidth. High-quality end-launch connectors would be required to reduce errors due to reflection and ensure repeatability.